REMARKS/ARGUMENTS

Claims 1-3, 8-10 and 15-17 are pending in the present application.

This Amendment is in response to the Office Action mailed June 29, 2004. In the Office Action, the Examiner rejected claims 18-21 under 35 U.S.C. §101 as a double patenting rejection; and claims 1-17 under 35 U.S.C. §102(e). Applicants have amended claims 1, 8, and 15. Reconsideration in light of the amendments and remarks made herein is respectfully requested.

Double Patenting

1. The Examiner rejects claims 18-21 under the statutory type double patenting of the claims in United States Patent No. 6,691,193. In response, Applicants would like to point out that claims 4-7, 11-14, and 18-21 were canceled in the preliminary amendment filed on November 12, 2003.

Accordingly, Applicants respectfully request that the Examiner withdraw the statutory type double patenting rejection.

Rejection Under 35 U.S.C. § 102

2. In the Office Action, the Examiner rejected claims 1-17 under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 6,260,093 issued to Gehman et al. ("Gehman"). In light of the cancellation of claims 4-7, 11-14, and 18-21 in the previous response, Applicants assume that the rejections apply only to claims 1-3, 8-10, and 15-17. Applicants respectfully traverse the rejection and contend that the Examiner has not met the burden of establishing a prima facie case of anticipation.

Gehman discloses a method and apparatus for arbitrating access to multiple buses in a data processing system. Master devices located on each of the buses are able to concurrently access resources on their individual bus (Gehman, col. 3, lines 44-46). When a master device accesses a resource located on a different bus, the transaction must cross a bridge (Gehman, col. 3, lines 46-49). The bridge then arbitrates for the bus and acts like a master device or target device on both buses (Gehman, col. 3, lines 49-58).

Gehman does not disclose, either expressly or inherently, at least (1) a slave access circuit to provide access to slave devices from a master processor; (2) a system bus controller interfacing to the master processors via master buses; and (3) the system bus controller dynamically mapping address spaces of the slave devices.

To anticipate a claim, the reference must teach every element of a the claim. "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." Vergegaal Bros. v. Union Oil Co. of California, 814 F.2d 628, 631, 2 USPQ 2d 1051, 1053 (Fed. Cir. 1987). "The identical invention must be shown in as complete detail as is contained in the...claim." Richardson v. Suzuki Motor Co., 868 F.2d 1226, 1236, 9 USPQ 2d 1913, 1920 (Fed. Cir. 1989).

In the Office Action, the Examiner states that Gehman teaches a slave circuit, slave devices, master processors, system bus controller, and a slave bus decoder (Office Action, page 3). Applicants respectfully disagree.

First, the Examiner states that Gehman discloses a slave access circuit as the bridge 112, 110, or 114 in Figure 1. However, the Examiner further states that Gehman discloses a system bus controller as bridge 112, 110, and 114. In other words, the Examiner identifies the bridge in Gehman as both slave access circuit and the system bus controller. In contrast, in the claimed invention, the slave access circuit is separate from the system bus controller. Furthermore, Gehman discloses that the bridge acts as a master device on one of the buses (e.g., bus 104) and a resource on another bus (e.g., bus 102) (Gehman, col. 3, lines 51-55). Therefore, the bridge cannot be a slave access circuit (which cannot act as a bus master), and cannot be the system bus controller (which maps address spaces of the slave devices) either separately or simultaneously.

Second, the Examiner states that Gehman discloses a system bus controller dynamically mapping address spaces of the P slave devices utilizing address decoders 130, 148, 132, and 140 to connect to resources. However, the decoders merely perform address decoding of the address issued by the master (Gehman, col. 3, lines 60-64), not mapping the address spaces of slave devices. Furthermore, this address decoding is not performed dynamically. The decoder merely selects either a device or another bridge depending on the address placed on the bus by the master device (Gehman, col. 5, lines 66-67; col. 4, line 1).

To clarify the claim language, independent claims 1, 8, and 15 have been amended.

Therefore, Applicants believe that independent claims 1, 8, 15 and their respective dependent claims are distinguishable over the cited prior art references. Accordingly, Applicants respectfully request the rejection under 35 U.S.C. §102(e) be withdrawn.

Conclusion

Applicant respectfully requests that a timely Notice of Allowance be issued in this case.

Respectfully submitted,

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